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H1A
Selected US specifications from IPC sub-class H01B

(54) High capacitance bus bar including multilayer ceramic capacitors

(57) A miniaturized bus bar comprises a polyimide sheet 18 laminated between a pair of bus conductors 12, 12', a plurality of multilayer ceramic capacitor elements 16 inserted in windows 20 and alternate conductive top and bottom electrodes (32, 34 Figs 2 & 3) of the capacitors electrically connected to the conductors 12, 12'. Conductive end plates (28,30) connect the internal electrodes of the capacitor to the top and bottom electrodes. Caps (36, 38 Figs 4 & 5) of glass or epoxy resin may be provided over the end plates. Electrical connections are made between the top and bottom electrodes (32, 34) to the bus conductors by solder (40 Fig 6) on projections on the conductors (44 Fig 7).

FIG. 1

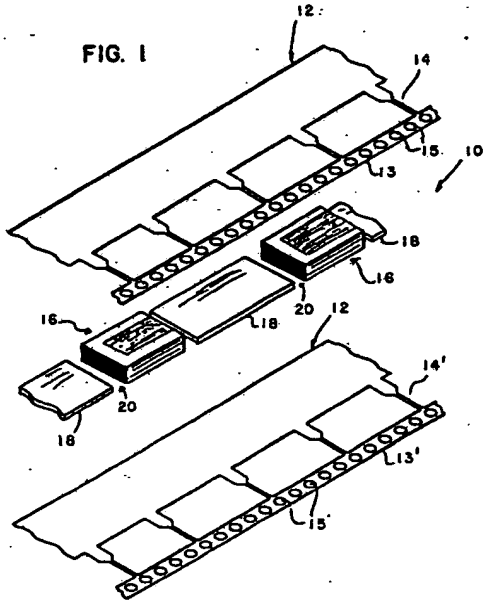

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FIG. 1

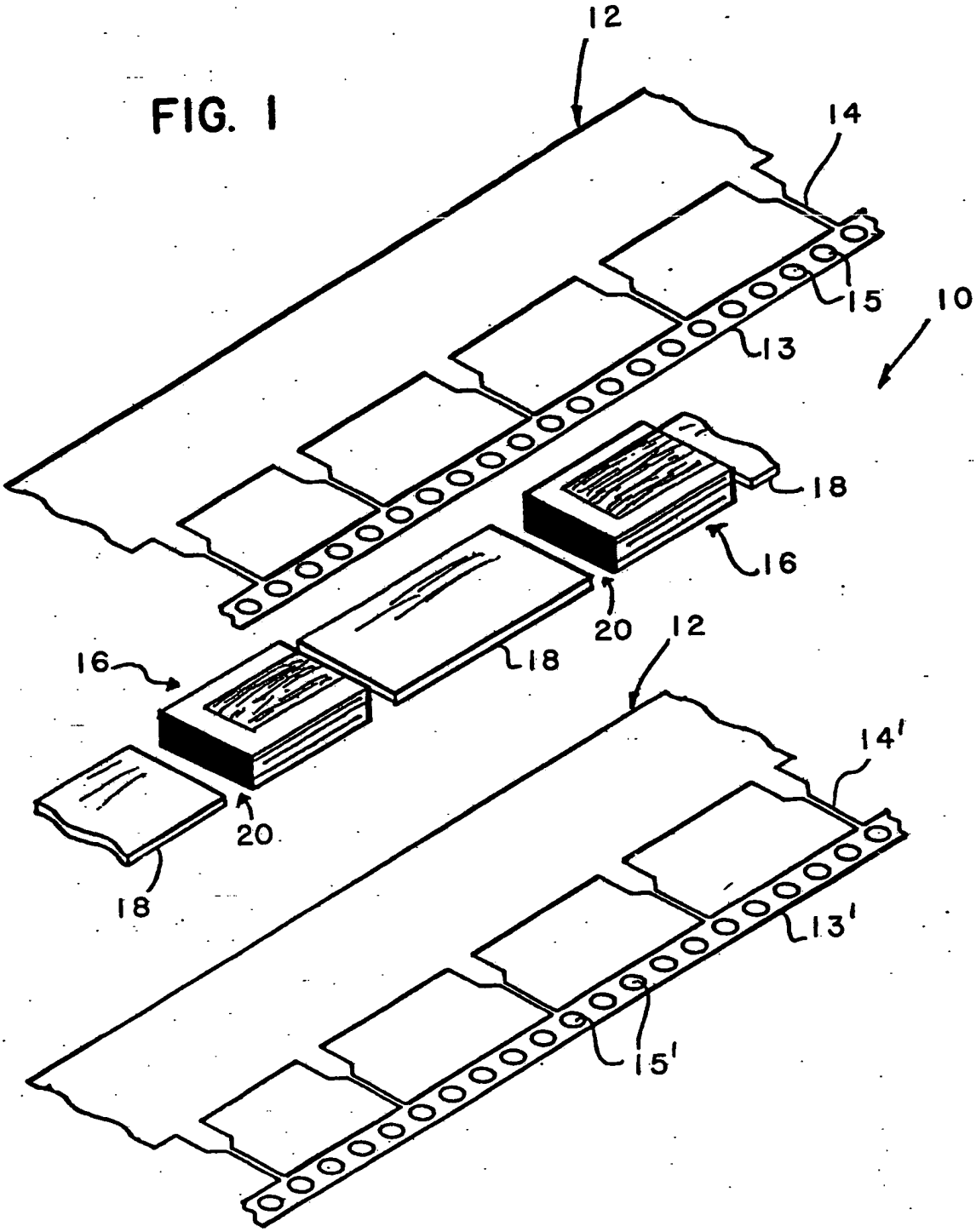

FIG. 2

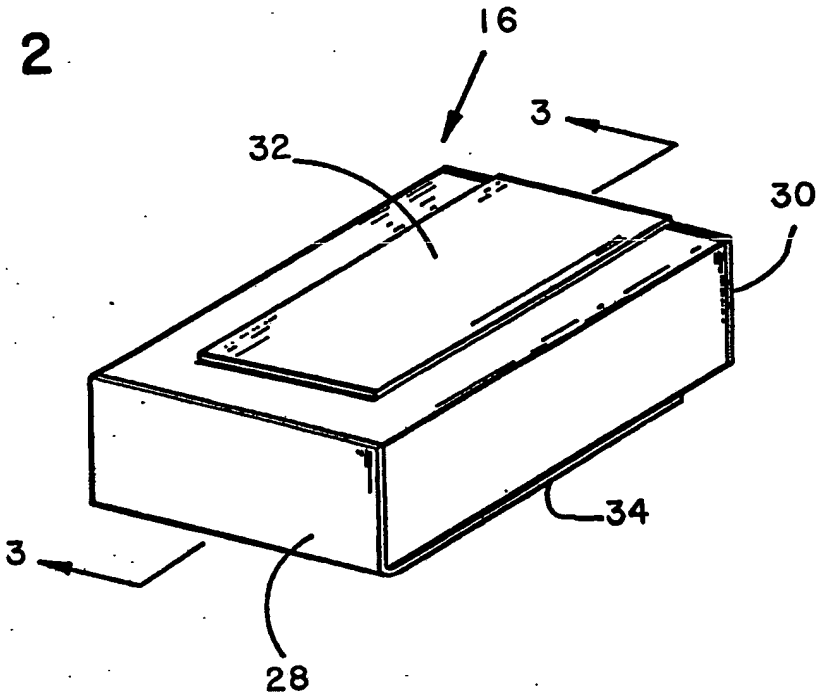

FIG. 3

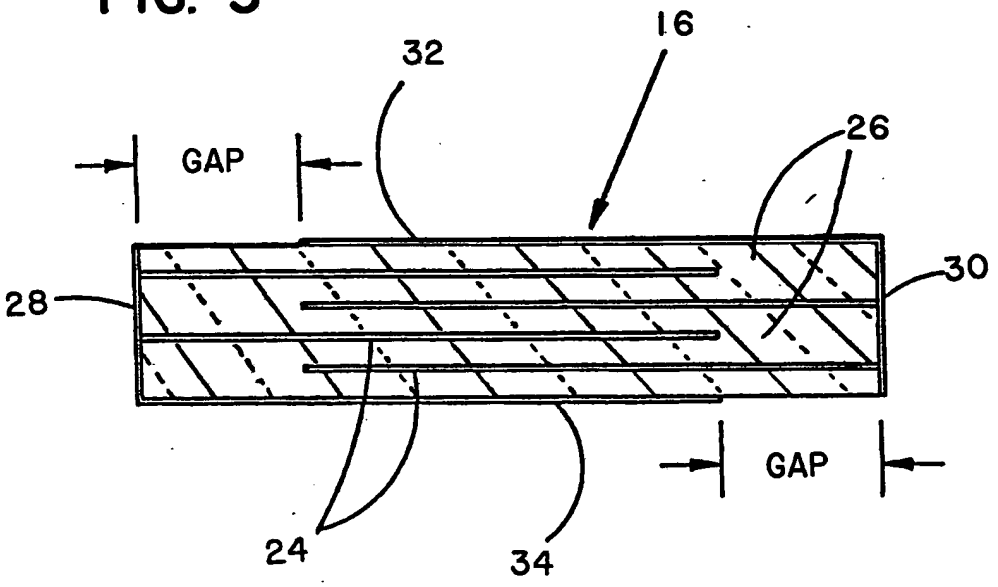

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FIG. 4

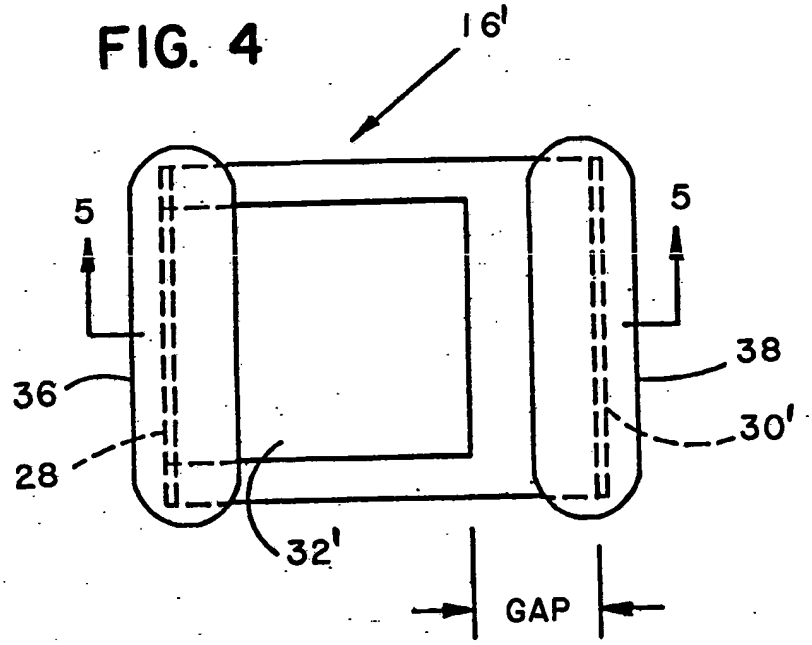

FIG. 5

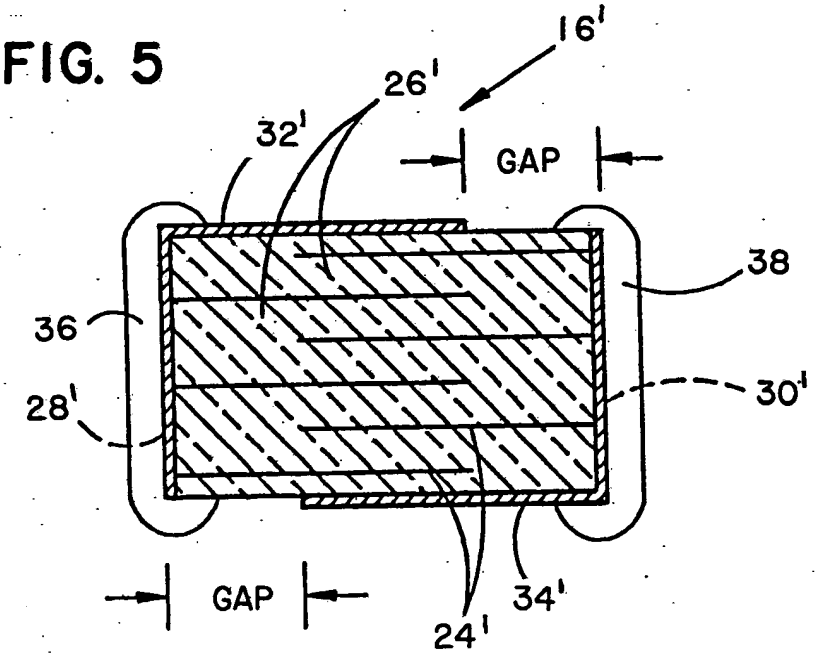

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FIG. 6

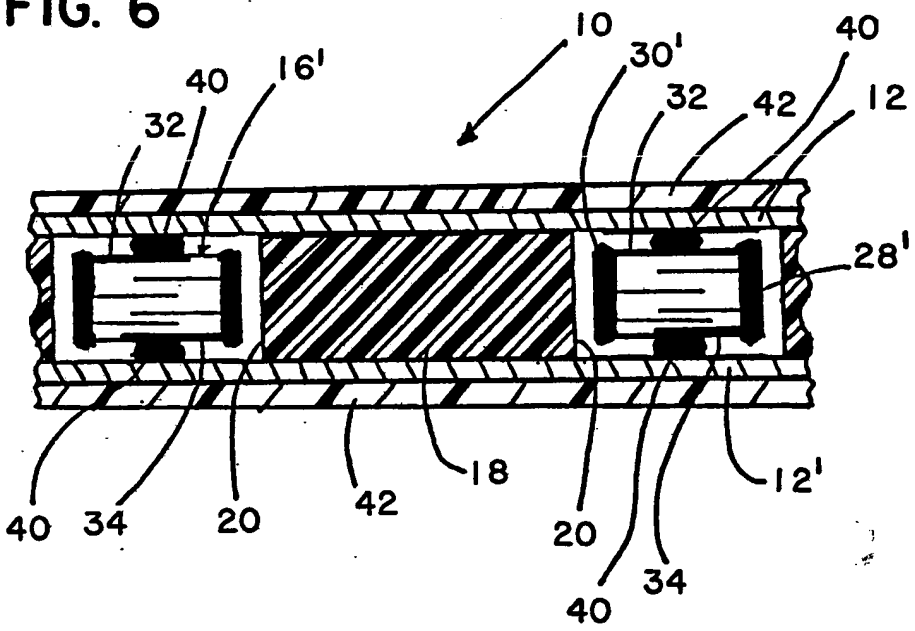
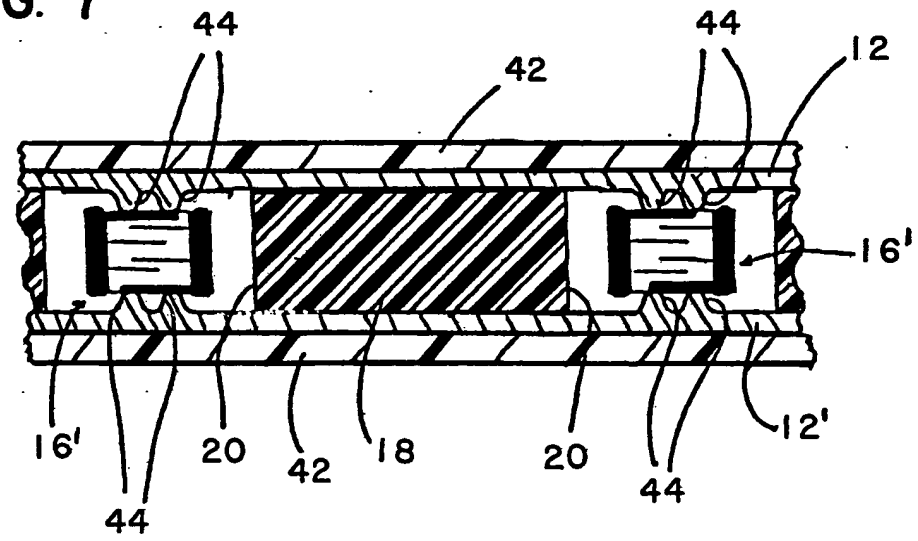


FIG. 7



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HIGH CAPACITANCE BUS BAR INCLUDING MULTILAYER CERAMIC CAPACITORS

This invention relates to bus bars and particularly to miniature bus bars having a high capacitance. More especially, this invention relates to novel bus bars which incorporate multilayer capacitive elements between pairs of elongated parallel bus conductors.

Conventional bus bars of relatively small or miniature size have been known in the art for a number of years. Such bus bar devices are used for power and/or signal distribution in many systems, such as, for example, computer back panels and integrated circuit systems. Such prior art multilayer bus bars, comprise at least two conductive plates (usually in the form of elongated strips or bars of copper) separated by an insulating film. Typically, the separating insulating layer is a plastic dielectric film such as a polyester material. The separator layer and the conductive plates are bonded together by an adhesive. Conventional prior art bus bars of this type have relatively low capacitance which results in the devices being comparatively ineffec-

tive in attenuating high frequency noise. This high frequency noise is highly undesirable, especially when the bus bar is used for signal distribution.

One prior art approach to eliminating this noise problem involves connecting capacitors to the bus bar after the completion of the bus bar assembly. While this approach raises the capacitance and minimizes the noise, it results in additional expense and time in manufacturing.

Another type of bus bar structure disclosed in the prior art involves disposing discrete high capacitive elements between a pair of conductors. These bus bars have the desired high capacitance. Examples of such high capacitance bus bars are disclosed in US Patent N°s 4,236,038; 4,236,046; 4,266,910; 4,342,881; 4,399,321; 4,403,108; 4,420,653; 4,436,953 and 4,599,486. The high capacitive elements utilized in those inventions are thin layers or chips of dielectric material, usually a ceramic with a high dielectric constant. The opposing surfaces of the chips are typically coated with a thin, integral and continuous film of conductive material and these conductive films are electrically connected to respective opposed surfaces of the bus conductors.

US Patent N°s 4,399,321 and 4,599,486 disclose the use of multilayer capacitor chips or elements having exposed electrodes at the ends or sides thereof. As a result, the exposed electrodes are actually transverse to the mutually parallel interleaved layers of metal and dielectric (i.e., ceramic) forming the monolithic capacitor chip. It has been found that such conventional multilayer capacitor chips suffer from certain deficiencies and drawbacks in terms of electrical operation due to increased inductance because of the non-parallel relationship between the end or side electrodes and the interleaved layers of metallization.

The purpose of the present invention is to overcome the above described and other problems of the prior art.

In accordance with the present invention, there is

provided a bus bar assembly comprising

insulating means, said insulating means being comprised of a flat elongated strip of non-conductive material having oppositely disposed first and second faces, said insulating means being provided with at least a first aperture extending therethrough between said faces;

a first bus bar conductor, said first bus bar conductor being bonded to said first face of said insulating means;

a second bus bar conductor, said second bus bar conductor being bonded to said second face of said insulating means;

said first and second bus conductors each including leads extending therefrom;

at least one multilayer capacitor means, said multilayer capacitor means being comprised of a dielectric material having a pair of opposed end surfaces and having top and bottom surfaces, said capacitor means having a plurality of parallel conductive layers interleaved within said dielectric material with alternating layers of conductive material being electrically connected and defining first and second groups of conductive layers, said first group having at least one exposed conductive layer on said top surface of said dielectric material defining a first exposed conductive layer and said second group having at least one exposed conductive layer on said bottom surface of said dielectric material defining a second exposed conductive layer, said capacitor means being positioned within said aperture of said insulating means with said first and second exposed conductive layers being oriented substantially parallel to said first and second bus bar conductors;

first means electrically connecting said first exposed conductive layer of said capacitor means to said first bus bar conductor; and

second means electrically connecting said second exposed conductive layer of said capacitor means to said

second bus bar conductor.

Certain embodiments of the invention will now be described, by way of example only, with reference to the drawings, wherein like elements are numbered alike in the several FIGURES:

FIGURE 1 is an exploded perspective view of a bus bar in accordance with the present invention;

FIGURE 2 is a perspective view of a multilayer ceramic capacitor element used in conjunction with the bus bar of FIGURE 1;

FIGURE 3 is a cross-sectional elevation view along the line 3-3 of FIGURE 2;

FIGURE 4 is a plan view of the multilayer ceramic capacitor element of FIGURE 2 with insulated caps;

FIGURE 5 is a cross-sectional elevation view along the lines 5-5 of FIGURE 4;

FIGURE 6 is a cross-sectional side elevation view of the bus bar of FIGURE 1 subsequently to assembly; and

FIGURE 7 is a cross-sectional side elevation view of another embodiment of a bus bar in accordance with the present invention.

Referring first to FIGURE 1, a portion of a miniature bus bar in accordance with the present invention, and prior to assembly and lamination, is shown generally at 10. Bus bar 10 includes a pair of elongated parallel bus conductors 12 and 12' from which project signal or power distribution pins or fingers 14 and 14', respectively. Bus conductors 12 and 12' are comprised of a conductive material (generally copper or copper alloy) and are usually manufactured by a stamping process. Preferably, bus bar 10 is manufactured in a continuous process wherein each bus conductor 12, 12' is attached to a lead frame or carrier strip 13, 13' via pins 14, 14'. Each carrier strip 13, 13' includes a plurality of registration openings 15, 15' for movement along a sprocket or the like.

A plurality of multilayer ceramic capacitor elements 16 or 16' are included within bus bar 10 between the two bus conductors 12 and 12'. A layer of insulating material 18, which may be comprised of a high temperature plastic mateial (such as a polyimide or a polyetherimide), is coated with an adhesive on both sides thereof and laminated between the two bus conductors 12 and 12'. Insulating spacer layer 18 is provided with registered openings 20 which define windows or pockets. Openings 20 are of the same shape and may be of the same size as the multilayer capacitor elements 16 or 16'. A capacitor element 16 or 16' is then positioned within each opening 20 as will be discussed in greater detail hereinafter.

Referring now to FIGURES 2-3, a multilayer chip capacitor element used in conjunction with the bus bars of the preferred embodiment is shown generally at 16. Capacitor element 16 is constructed of a series of conductive layers 24 separated by layers 26 of a material having a high dielectric constant. The dielectric material will, in accordance with the preferred embodiment, be a ceramic such as barium titanate. Each conductive layer 24 had only one of its ends exposed at a side of element 16, with alternate conductive layers 24 having exposed ends at the same side of element 16. The pair of opposed end faces of element 16, to which conductive layers 24 extend, are metallized whereby conductive end plates 28 and 30 are defined; the groups of alternating conductive layers 24 being in electrical contact with end plates 28 and 30. Significantly, and as will be discussed in more detail hereinafter, multilayer capacitor element 16 has its outermost electrodes 32 and 34 exposed to define top (electrode 32) and bottom (electrode 34) connecting surfaces.

Referring again to FIGURES 2-3, while suitable for its intended purposes, multilayer capacitor chip (MLC) 16 as shown therein can suffer from a disadvantage with regard to the conductive adhesive or solder (see FIGURE 6) used to electrically and mechanically connect

electrodes or conductors 32 and 34 to bus bar conductors 12 and 12', respectively. Typically, MLC 16 is quite small in size (about 3 mm x 4,5 mm or 3,8 mm x 7,6 mm and between 0,33 mm x 0,5 mm in thickness). Consequently, as shown in FIGURE 3, the chances of conductive adhesive or epoxy covering or bridging one or both of the gap's between electrodes 32 and 34 thus producing a short circuit are quite good. There is also a likelihood of electrical contact between bus conductors 12 and 12', and end terminations 28 and 30 (see FIGURE 6). It will be appreciated that this electrical contact will also produce a short circuit.

Turning now to FIGURES 4 and 5, in a preferred embodiment, the multilayer capacitor element used in accordance with the present invention is shown generally at 16' and is provided with an insulating cap 36 and 38 surrounding and encapsulating the end terminations 28' and 30' of conductors 32' and 34', respectively. It is apparent that insulative caps 36 and 38 prevent any electrical bridging in the gaps between electrodes 32' and 34' (in contrast to MLC 16 in FIGURES 2-3). As a result, the possibility of electrical shorting between electrodes 32' and 34' is eliminated, as well as the possibility of shorting between the bus conductors 12 and 12' and the end terminations 28 and 30 of FIGURE 3.

Insulative caps 36 and 38 may be comprised of any suitable electrically insulative material including glass or epoxy. Preferably, the insulating material should provide a hermetic seal, good adhesion and high voltage breakdown.

In a preferred method of making MLC 16', even numbers of ceramic sheets 26' with screened electrode patterns 24' are laminated together such that the external planes expose electrodes 32' and 34'. The laminates are then cut into individual chips and fired. After firing, a thin, preferably silver end termination 28' and 30' (band width less than 0,12 mm) is applied and fired. A second end termination 36 and 38 of dielectric

glass is then applied (band width approximately 0,38 mm) which coats and insulates the silver end terminations 28' and 30'. The glass is then fired to yi ld a finished chip. Thus, end terminations 28' and 30' essentially interconnect alternating conductive sheets 24' with the outer conductive sheets 32' and 34' defining upper and lower electrodes. In FIGURE 6, the preferred MLC 16' of FIGURES 4 and 5 is shown after assembly in a bus bar 10. As is evident from the FIGURES, conductive adhesive is precluded from bridging the gap between electrodes 32' and 34' by insulated coatings or end caps 36 and 38.

As previously discussed, conventional multilayer ceramic chip capacitors have utilized exposed electrodes at either end rather than the top and bottom electrode configuration of FIGURES 2-5. Such a conventional prior art MLC is shown generally at 68 in FIGURE 13 of EP-A-0200670.

An important feature of the present invention is that the electrical properties, particularly the inductance of the bus bar, is greatly improved relative to prior art constructions such as are shown in US patent N°s 4,399,321 and 4,599,486. It will be appreciated that the important improved electrical performance of the present invention is not obtainable using a parallel plate bus bar construction in conjunction with a conventional MLC such as is shown in FIGURE 13 of EP-A-0200670. This is because MLC 68 of FIGURE 13 utilizes electrodes at either end (rather than top and bottom) which preclude a parallel plate construction. Only by using the novel MLC 16 and 16' wherein the electrodes are positioned along the top and bottom (and are therefore parallel to the interleaved metallization 24 and 24') may the improved electrical performance (i.e., lower inductance) be achieved.

As mentioned, the multilayer ceramic capacitor element shown in FIGURES 2-5 has a novel configuration relative to the multilayer capacitor chips generally used in prior art high capacitance miniature bus bars. This

difference stems from the conductive layers 24 being exposed at the top and bottom of the element 16 for attachment to bus conductors 12 and 12' rather than being exposed at the ends of the capacitor element for connection to conductive end plates. For example, in prior art US patent N° 4,399,321, the capacitor element disclosed therein utilizes a conventional multilayer capacitor wherein the conductive layers are exposed at the ends thereof and conductive end plates are used which eventually connect to the pair of elongated bus bar conductors. As a result, the exposed electrodes of the MLC of Patent N° 4,399,321 are transverse both to the bus conductors and to the internal metal layers within the capacitor, per se. Similarly, in prior US Patent N° 4,599,486, the exposed electrodes are located along the sides of the multilayer capacitor. While the electrodes of Patent N° 4,599,486 will be parallel to the bus conductors (unlike the multilayer capacitor of Patent N° 4,399,321), the side electrodes will still be transverse to the interleaved metal layers within the capacitor. This is in distinct contrast to the present invention wherein the top and bottom electrodes will be mutually parallel to both the bus conductors and the internal metal layers within the capacitor, per se.

Turning now to FIGURE 6, as mentioned, the conductive layers 12, 12' and insulating layer 18 are assembled together with the proper fixturing and then hot press laminated to form a permanent laminate structure. Windows or slots 20 are formed through insulating layer whereupon the multilayer capacitor elements 16, 16' are inserted through the slots. An important feature of the present invention is that the conductive top and bottom electrodes 32 (32') and 34 (34') of multilayer capacitor elements 16 (16') are oriented such that they electrically contact the respective bus conductors 12 and 12'. Stated differently, the conductive top and bottom electrodes 32 (32') and 34 (34') on the capacitor elements 16 (16') are inserted through openings 20 so

that they will be parallel to bus conductors 12, 12' and to metal layers 24 (24') in capacitor element 16 and 16'. This is in distinct contrast to prior art bus bars such as those disclosed in US Patent N°s 4,399,321 and 4,599,486 wherein the conductive end or side plates of those capacitor elements are oriented perpendicular to the bus conductors and/or metal layers of the multilayer capacitor elements.

After capacitor elements 16 or 16' have been inserted into slots 20, solder paste or a similar electrical adhesive (i.e., conductive epoxy) material is applied to both conductive top and bottom electrodes 32 and 34 in the area of window 20. The solder paste or other adhesive is shown generally at 40 in FIGURE 6. The solder paste or conductive adhesive is then reflowed (or cured) to effect strong mechanical and electrical contact between top and bottom electrodes 32 and 34 and bus bars 12 and 12', respectively. Following such a reflow or curing process, the assembly is cleaned using any appropriate and well known method.

Preferably, the miniature bus bar assembly is then encapsulated or insulated by any suitable method (such as dipping, fluidized bed coating, electrostatic spray, etc.) to provide environmental protection and prevent shorting. Also in a preferred embodiment, leads 14, 14' will not be covered with an encapsulating or insulating layer so as to provide improved soldering to the printed wiring board. An encapsulating or other insulating layer or sheath is shown generally at 42 in FIGURE 6.

Turning now to FIGURE 7, rather than electrically connecting top and bottom electrodes 32 and 34 to bus bar conductors 12 and 12' using conductive adhesive (i.e., solder or conductive epoxy), in an alternative embodiment, electrical connection may be effected by formation of dimples or crimps 44 in bus conductors 12 and 12'. Thus, electrical contact between multilayer capacitor lement 16 or 16' and conductor 12 and 12' is made by the dimples 42 contacting the electrodes 32 and 34 of the

MLC. This electrical contact will be maintained by compressive forces wherein dimples 42, 42' will be urged against electrodes 32' and 34', respectively during the lamination process.

It will be appreciated that the degree of capacitance in a bus bar constructed in accordance with the present invention will depend upon the number of capacitive elements used in the bus bar as well as the amount of capacitance for each multilayer capacitor element used therein.

CLAIMS

1. A bus bar assembly comprising :

insulating means, said insulating means being comprised of a flat elongated strip of non-conductive material having oppositely disposed first and second faces, said insulating means being provided with at least a first aperture extending therethrough between said faces;

a first bus bar conductor, said first bus bar conductor being bonded to said first face of said insulating means;

a second bus bar conductor, said second bus bar conductor being bonded to said second face of said insulating means;

said first and second bus conductors each including leads extending therefrom;

at least one multilayer capacitor means, said multilayer capacitor means being comprised of a dielectric material having a pair of opposed end surfaces and having top and bottom surfaces, said capacitor means having a plurality of parallel conductive layers interleaved within said dielectric material with alternating layers of conductive material being electrically connected and defining first and second groups of conductive layers, said first group having at least one exposed conductive layer on said top surface of said dielectric material defining a first exposed conductive layer and said second group having at least one exposed conductive layer on said bottom surface of said dielectric material defining a second exposed conductive layer, said capacitor means being positioned within said aperture of said insulating means with said first and second exposed conductive layers being oriented substantially parallel to said first and second bus bar conductors;

first means electrically connecting said first exposed conductive layer of said capacitor means to said first bus bar conductor; and

s cond means electrically conn cting said second

exposed conductive layer of said capacitor means to said second bus bar conductor.

2. A bus bar assembly as claim d in claim 1, wherein said capacitor means further includes :

a first conductive end termination on one of said opposed end surfaces of said dielectric material and a second conductive end termination on the other of said opposed end surfaces of said dielectric material;

said first group of conductive layers terminating at said first conductive end termination and said second group of conductive layers terminating at said second conductive end termination, said first exposed conductive layer being connected and substantially transverse to said first conductive end termination, said second exposed conductive layer being connected and substantially transverse to said second conductive end termination, a first gap being defined between said first exposed conductive layer and said second end termination and a second gap being defined between said second exposed conductive layer and said second end termination.

3. A bus bar assembly as claimed in claim 2, wherein said capacitor means further includes :

an electrically insulative cap being provided over each of said first and second conductive end terminations wherein said conductive end terminations are encapsulated and wherein electrical bridging in said gap between said first exposed conductive layer and said second conductive end termination and in said gap between said second exposed conductive layer and said first conductive end termination is precluded by said insulative cap.

4. A bus bar assembly as claimed in claim 3, wherein :

said insulative cap is comprised of a material selected from the group comprising glass and exopy.

5. A capacitor as claimed in any preceding claim wherein: said dielectric material is a ceramic material.

6. A bus bar assembly as claimed in any preceding claim wherein: said first and said second electrical connecting

means is solder.

7. A bus bar assembly as claimed in any of claims 1 to 5, wherein said first and said second electrical connecting means is conductive adhesive.

8. A bus bar assembly as claimed in any of claims 1 to 5, wherein said first and second electrical connecting means are dimples formed in said first and said second bus bar conductors.

9. A bus bar assembly as claimed in any preceding claim, further including :

sheath means, said sheath means being non-conductive, said sheath means insulating at least a portion of said first and said second bus bar conductors and said capacitor means.

10. A bus bar substantially as hereinbefore described with reference to any one or more of the accompanying drawings.

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